What is claimed is:

1. A method for fabricating a non-volatile memory device, the method comprising:

forming at least a pair of floating gate lines on a semiconductor substrate, the pair of floating gate lines defining a gap therebetween;

etching a portion of the substrate between the pair of floating gate lines to form a trench therein;

forming a gap-fill dielectric layer in the trench and also in the gap; and

implanting the gap-fill dielectric layer.

2. The method of claim 1, further comprising:

forming an inter-gate dielectric layer on the floating gate lines and on the gap-fill dielectric layer;

forming a conductive layer over the inter-gate dielectric layer; and

patterning the conductive layer and the floating gate lines to form a word line and a floating gate.

3. The method as recited in claim 1, wherein implanting comprises using phosphorous ions.

4. The method as recited in claim 3, wherein implanting is performed at a dose of about 1.0×10^{13} ions/cm^2 or greater and at an energy level of about 100 KeV or less.

5. The method as recited in claim 1, wherein implanting is performed so that the projection range (Rp) of implantation is located in the vicinity of the floating gate.

6. The method as recited in claim 1, wherein the gap-fill dielectric layer is a CVD oxide.

7. The method as recited in claim 1, further comprising implanting the substrate adjacent to the word line to form source/drain regions.

8. A method for fabricating a non-volatile memory device, the method comprising:

forming at least a pair of lower floating gate lines on a substrate having a tunnel dielectric layer formed thereon, the pair of lower floating gate lines defining a gap therebetween;

forming a polishing stop layer pattern on the lower floating gate lines;

etching a portion of the substrate between the pair of lower floating gate lines to form a trench therein;

forming a gap-fill dielectric layer in the trench and also in the gap;

removing the polishing stop layer pattern to expose surface of the pair of lower floating gate lines;

forming a upper floating gate conductive layer on the exposed lower floating gate lines and on the gap-fill dielectric layer;

forming a hard mask layer pattern on the upper floating gate conductive layer;

etching a portion of the upper floating gate conductive layer, until the gap-fill dielectric layer is exposed, to form upper floating gate lines on the lower floating gate lines, using the hard mask layer pattern as an etch mask;

removing the hard mask layer pattern;

forming an inter-gate dielectric layer on the upper floating gate lines and on the gap-fill dielectric layer;

forming a conductive layer on the inter-gate dielectric layer;

patterning the conductive layer, the upper floating gate lines, and the lower floating gate lines to form a word line and a floating gate; and

implanting the gap-fill dielectric layer with impurities.

9. The method as recited in claim 8, wherein implanting is performed by using phosphorous ions.

10. The method as recited in claim 8, wherein implanting is performed at a dose of about 1.0×10^{13} ions/cm^2 or greater and at an energy level of about 100 KeV or less.

11. The method as recited in claim 8, wherein implanting is performed so that the projection range (Rp) of implantation is located in the vicinity of the floating gate.

12. The method as recited in claim 8, wherein implanting is performed after forming a gap-fill dielectric layer in the trench and the gap between the lower floating gate lines and before removing the polishing stop layer pattern.

13. The method as recited in claim 8, wherein implanting is performed after removing the polishing stop layer pattern and before forming the upper floating gate conductive layer.

14. The method as recited in claim 8, wherein implanting is performed after etching the upper floating gate conductive layer using the hard mask layer pattern and before removing the hard mask layer pattern.

15. The method as recited in claim 8, wherein implanting is performed after removing the hard mask layer pattern and before forming the inter-gate dielectric layer.

16. The method as recited in claim 8, further comprising forming spacers on sidewalls of the hard mask layer pattern.

17. The method as recited in claim 8, wherein the upper floating gate lines overlap a portion of the gap-fill dielectric layer.

18. The method as recited in claim 8, wherein the gap-fill dielectric layer is a CVD oxide.

19. The method as recited in claim 8, further comprising implanting the substrate adjacent to the word line to form source/drain regions.